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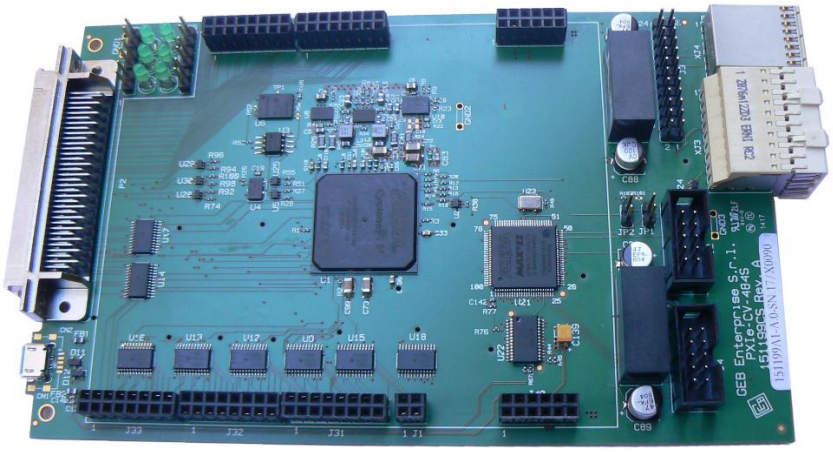
SOPC
System On Programmable Chip

PXI Express: PXIE-CV

The PXIe FPGA card joins the powerfully of the PXI express standard to the flexibility and high performance of a cyclone V FPGA. The FPGA board is a carrier that bring inside the high performance of the PCIE bus up to its daughter board hosted on the its expansion connectors

Features

• PXI-E 3 U size Peripheral Function		
Available in two FPGA configuration:		
Resource	EP5CGXC3	EP5CGXC5
• Logic elements	35500	77000
• Ram (Kbits)	1540	29080
• PCI Express IP	GEN1X1	1X4
• PLLs	4	6
• 18x18bit multi.	114	300
• Expansion Daughter board can be hosted on header connectors		
• 52 LVTLL (2.5, 3.0, 3.3V) FPGA I/O Available on Daughter connectors		
• 16 LVTLL (2.5, 3.0, 3.3V) FPGA I/O Available on front connector		
• 32 I/O with customized electrical level by customized daughter board		
• Allows fpga boot from PXIe		
• Allows fpga boot programming from USB micro connector on front panel		
• On board crystal oscillators provides accurate clock reference.		
• Preloaded FPGA firmware make available expansion bus IP, GPIO a DMA.		
• On board USB blaster allows on field fpga programming		
• Fully compatible with JTAG/IEEE 1149.1 boundary-scan standard.		



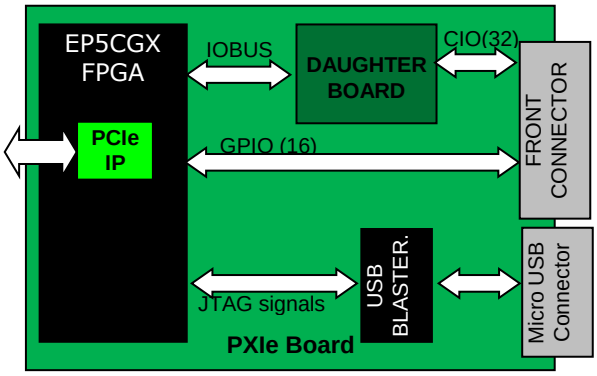
Description

GEB High Performance PXIe fpga board includes whatever needed for using the advanced features of Altera CycloneV-GX hosting on the boards a large set of fpga starting from the cheaper one with its 35KLE up to the biggest on that allows 114KLE.

The board architecture has been thought to be used in equipment where the building of an application in short time with low non-recurring costs are strongly needed. The FPGA interfaces the board to the PXIe slot trough the PCIe interfaces and some PXIe specific signals such as the PXIE TRIG.

The Fpga can drives the interfaces the application in 2 ways:

- Using a straight way through 16 GPIO signals (USR0-15) that are brought out wired by the 68 way male connector on the front panel. The signals have been made tolerant to 5V TTL logic trough some onboard level translators.
- Through a daughter board that can hosted on some dedicated header connectors. It allows many custom I/O with user selected levels and protocols. 32 of them (CIO) can be brought out to the front connector through two dedicated header connectors.



The USB blaster supports in system programming and debugging by PXIs controller USB port. It allows remote FPGA reconfiguration and remote on field issues fixup.

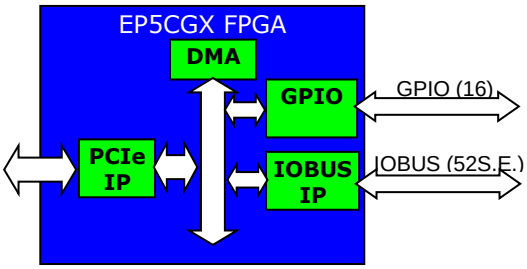
Application

The typical applications are test equipment for production and qualification, engineering test bench, automatic measurement system, electronic equipment that support chemistry, nuclear physics experiments. The flexibility of FPGA and the uses of the daughter board allow the interfacing of your custom application in fast and cheaper way.

PXIe-IOBUS-GPIO Fpga system

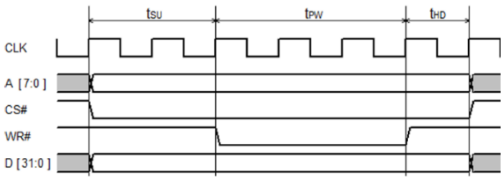
The fpga system is optionally supplied programmed on the board allowing its uses immediately. The system includes:

- One PCI express Interface GEN1X1,
- Scatter Gather Direct Memory Access (SGDMA) controller. It allows DMA from/to PC virtual memory from/to local I/O.
- One IoBus timing programmable bus interfaces. It allow to manage up to 24 address bits, up to 32 data bits
- Four PIO, each with 8 bidirectional bits. Each bit can be individually programmed and can work in "edge capture" mode and generate an interrupt.
- Source and compiled files (targeted on 151199A1)
- MS windows seven drivers and examples.



The IOBUS IP and PIN sharing

The IOBUS allow to manage up to 32 address bits, up to 32 data bits, 2 chip select, READ and WRITE controls, 1 interrupt (IRQ) and a wait/ready (WAIT) signal. The IP would use 68 fpga pins to bring out all its signals. Note that the timing, in terms of RD/WR pulse width, address and data setup and hold, control signal polarity are programmable



There are also four PIO, two of them are wired to the front panel connector through 16 pins, the others two would need 16 extra pins. Adding the IOBUS and PIOS pin 82 pins will be needed over 52 that have been available. In the compiled example a software programmable mux will allow selecting of which pin will be bring out. The default configuration will bring out 15 Address, 16 Data, 2 CS#, 1 IRQ, RD#, WR#, and 16 PIO bits.
Obviously, starting from QuartusII design and sources, you'll customize the application inserting your needed logic between the IOBUS or PIO signals and the FPGA pins.

PXI specific signals

The Fpga can handle some PXI specific signals to perform events synchronization and others similar instrumentation actions. The signals wired to the fpga are PXI_TRIG 0..7, PXI_LBL6, PXI_LBR6, PXI_CLK10 e PXIe_SINC100+/- that have replaced on the PXIe connector the similar PXI signals that have become not available now.

FPGA Programming and Debug.

The Fpga can be programmed in two ways:

- Using the standard methods trough an onboard USB Blaster. It will be enough a simple USB to micro USB cable from an USB hosted on the CPU and the micro USB connector hosted on the PXI-CV-484 front panel. Using the classic Altera programmer, you'll configure the FPGA boot flash. Using the same methods, you'll debug your application by Signal Tap.
- The second method adds a great flexibility allowing the FPGA boot by PXIe bus trough the Configuration Via Protocol (CVP) supported by Altera Cyclone V devices. It allows considering the FPGA a part of the application software following its configuration tools and history. The designer must pay attention to design structure using logic lock to meet the CVP requirements.

Specifications and Operating Conditions

Operative temperature range	0+70°C Commercial Temp. Range (*1)
Storage temperature range	-40/+150°C

Notes: (*1) The operative temperatures assumes an FPGA Tja=15°C. Tja depends from FPGA power dissipation. Boards in Industrial Temperature Range can be bought but are out of stock, please contact GEB Enterprise for their delivery time

Ordering Information

Product Name	GEB Code	Description
PXIe-CV-484/C3	151199A1	PXIe board equipped with EP5CGXFC3B7F23C8
PXIe-CV-484/C5	151199A2	PXIe board equipped with EP5CGXFC5C7F23C8
PXIe-IOBUS-GPIO	160401A1	FPGA System with PCI express IP GEN1X1, 1 Dma Controller, 1 IoBus bus interfaces, 4 PIO with 8 bidirectional bits. Source and compiled files (targeted on 151199A1) completed of MS windows seven drivers.

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