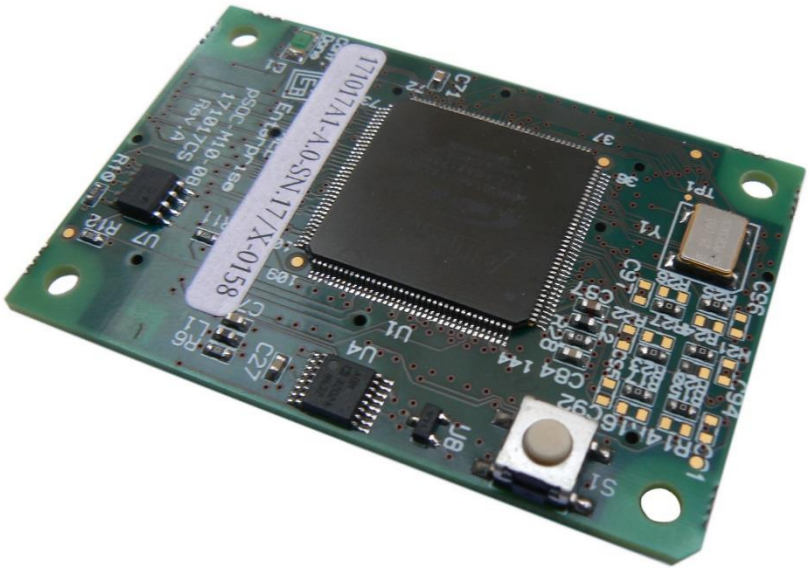
pSoc-M10

USER'S MANUAL



DOCUMENT REVISION HISTORY

Rev.	Date	Description
A	15/12/2017	First Release
B	30/01/2018	Change PCB revision, (Pin Mapping)

Emission Date	30/01/2018	Resp. PRG		Resp. RSQ	

INDEX

INDEX of FIGUREs

INDEX of TABLEs

1. Introduction

The **pSoc-M10** is a Max 10 development board for various applications, providing 52 general purpose I/Os in a small form factor.

All FPGA power management, distribution and decoupling, fine pitch EQFP package connection, multilayer PCB manufacturing, double side PCB mounting and testing requirements are met by pSoc board.

Figure 1: pSoc-M10-08 board top view.

The hardware design can be easily implemented using QSYS Altera tools, VHDL language, or a combination of them.

The Board support System with NIOS II able to run simple application written in c, using the various peripheries available on QSYS, in a simple development environment powered by Eclipse

The 50 mills header connectors allows to easily interface user boards

1.1. TECHNICAL FEATURES

- MAX10 Fpga TQFP144 footprint can Host from 10M08 up to 10M50 Fpga, upto:
  - 50KLE
  - 1638 Kbytes Memory (Ram or Rom)
  - 746 Kbytes user Flash
  - 144 18 bits Multipliers
- Single 3.3V power supply voltage
- 51 general purpose I/O pins, 3.3V LVTTL compliant, each one having independent sense, drive, bi-directional, and tri-state capabilities
  - 5 shared with SPI
  - 6 can operate as ADC inputs with optional RC filters
  - 5 can operate as clock out
- JTAG/IEEE 1149.1 boundary-scan standard full-compatibility
- 25 MHz on-board oscillator
- Power on monitor and reset circuitry
- 2 Mbytes SRAM
- 1 reset push button
- 1 Power monitor and Reset
- Board Size 60x40x8mm

1.2. VOLTAGE LEVELS AND WORKING TEMPERATURES

The following table reports power supply and temperature values of the **PSoc-M10** board:

Digital I/O	Vol=0.4V max., Voh=2.4V min., Vil=0.8V max., Vih=2.0V min.
Power supply (current)	3.3V+/- 5% (0.25A Typical, 0.6A Max)[1]
Operating Temperature Range	Tj 0°C/+85°C Commercial Temp. Range, Tj -40°C/+100°C Industrial Temp. Range[2]
Storage Temperature Range	-40/+150°C

Table 1: Voltage levels and working temperatures.

[1] The current value depends from the configuration file loaded inside FPGA. The typical values was measured on typical application (100MHz system clock, 50% resource usage, 20% I/O switching at 10MHz). Maximum value was estimated using Altera tolls in many large and fast design. The maximum current values allowed depends also from the thermal resistance of the package and from the operating temperature.

[2] The operative temperatures assumes an FPGA Tja=15°C. Tja depends from FPGA power dissipation. Available on request.

2. BLOCK DIAGRAM

The following figure shows the block diagram of the **PSoc-M10** board:

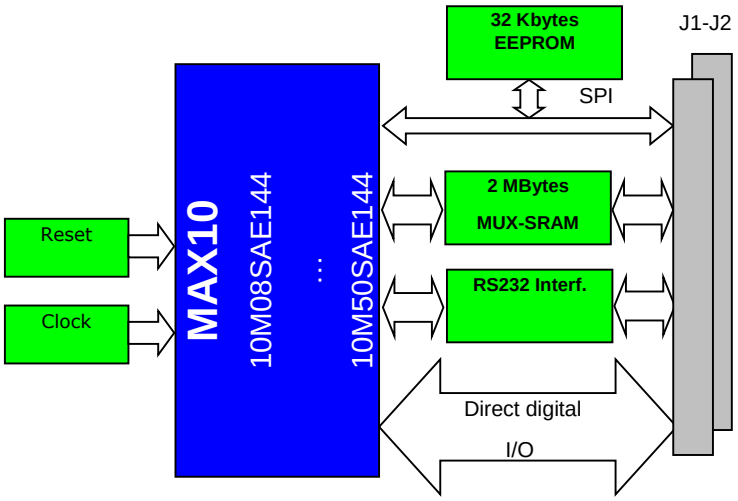


Figure 2: Block diagram of the PSoc-M10 board.

3. MAX 10

The following table reports the technical features of MAX 10 FPGA SA EQFP 144 version, that can be hosted on the PSoc-M10 board:

Fpga Type	10M08SA	10M16SA	10M50SA
Logic Elements	8,064	15,840	49,760
Total RAM Bits	387 Kbits	549 Kbits	1638 Kbits
Total User Flash Bytes	172 KB	296 KB	11.534 KB
PLLs	1	1	1
ADC	1	1	1
Multipliers Blocks	24	45	144
Maximum user I/O pins	101	101	101
Package	EQFP144	EQFP144	EQFP144
Speed Grades	-6, -7, -8	-6, -7, -8	-6, -7, -8
Fewe Support	NONE	NONE	NONE

Table 2: Technical features of the hosted MAX 10 FPGA.

4. CLOCKING AND RESET

The **PSoc-M10** board provides a free running 25 MHz oscillator, which drives the FPGA directly. Moreover, an input user provided clock and a PLL output clock signals are available to the user via the J1 connector: refer to section 6.2 for further details.

A low-active reset signal is connected to the INIT_DONE pin of the FPGA (configured as output open drain), and it is normally high due to a pull-up. The user can provide an extra low-active reset signal via the J1 connector, as shown in section 6.1.

Table 3 summarizes the clocking and reset scheme just described.

Signal name	Description	FPGA location
REF_CLK	On-board oscillator 25 MHz clock signal	26
FPGA_RSTn	FPGA low-active reset signal	121

Table 3: On-board clock and reset signals summary.

5. SRAM signal Pin

The **PSoc-M10** board provides a 2 MBites Static Ram with multiplexed Data an Address Line.

Table 4 summarizes the SRAM Signals name and the corresponding Pin of FPGA

Function	PIN FPGA	PIN FPGA	Function
AL[0]	21	135	AD[9]
AL[1]	39	132	AD[10]
AL[2]	41	130	AD[11]
AL[3]	112	127	AD[12]
AD[0]	141	122	AD[13]
AD[1]	136	119	AD[14]
AD[2]	134	113	AD[15]
AD[3]	131	43	BEn[0]
AD[4]	124	44	BEn[1]
AD[5]	38	25	RDn
AD[6]	120	56	WRn
AD[7]	114	24	Csn
AD[8]	140	102	ALE

Table 4: On-board clock and reset signals summary.

6. . I/O CONNECTIONS

The **PSoc-M10** development board provides two general purpose I/O connectors for user purposes, like for example LEDs, switches, ASSPs, and so on.

6.1. J1 connector

Figure 3 shows the J1 connector with pin numbers and signals:

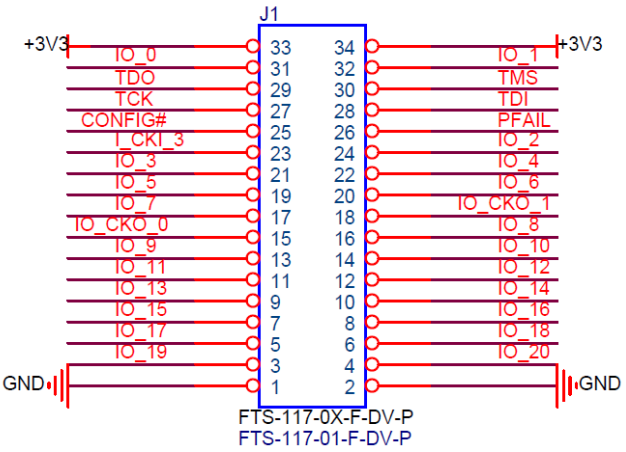


Figure 3: J1 connector.

As it can be seen, 24 general purpose I/O pins are provided on the J1 connector. Moreover, a POWER signal and 6 further specific signals are provided. These signals are described in Table 5:

Signal name	Description
TDO,TDI,TMS,TCK	JTAG Signals
CONFIG#	JTAG Enable signal (LOW)
PFAIL	Power Fail signal

Table 5: J1 connector specific signals description.

The following table shows the mapping between the FPGA pin locations and the J1 connector pins number and function:

Function	PIN FPGA	Pin number	Pin number	PIN FPGA	Function
+3V3	-	33	34	-	+3V3
IO_0/ADCIN2	6	31	32	7	IO_1/ADCIN3
TDO	20	29	30	16	TMS
TCK	18	27	28	19	TDI
CONFIG#	129	25	26	27	PFAIL
IO_CKI_3	28	23	24	17	IO_2
IO_3/ADCIN4	8	21	22	9	IO_4/ADCIN5
IO_5/ADCIN7	10	19	20	11	IO_6/ADCIN8
IO_7	30	17	18	33	IO_CKO_1
IO_CKO_0	32	15	16	45	IO_8
IO_9	48	13	14	47	IO_10
IO_11	50	11	12	52	IO_12
IO_13	54	9	10	55	IO_14
IO_15	57	7	8	58	IO_16
IO_17	59	5	6	60	IO_18
IO_19	62	3	4	64	IO_20
GND	-	1	2	-	GND

Table 6: J1 connector pins function and mapping.

The IO/ADCINx pins can be the Input of ADC (if enabled), this have the Optional RC Filter only in the A2 and A3 Version of pSOC Board.

6.2. J2 connector

Figure 4 shows the J2 connector with pin numbers and signals:

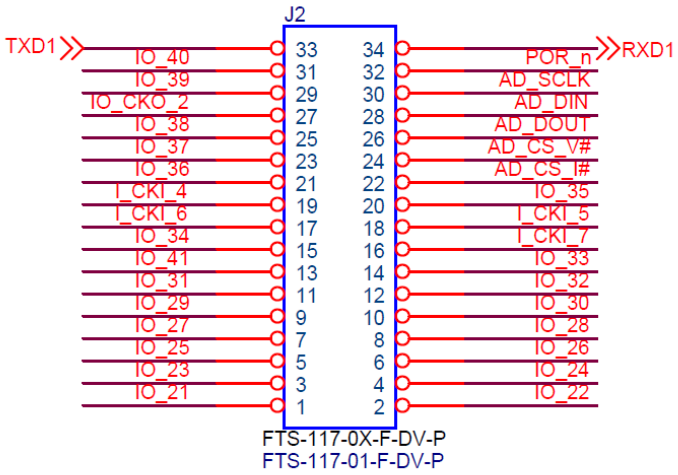


Figure 4: J2 connector.

As shown in the figure above, in addition to 26 general purpose I/O signals and 8 further specific signals are provided. These signals are described in Table 7:

Signal name	Description
AD_xx	SPI Interface Signals
POR_n	Reset Signal (Active LOW)
TXD1, RXD1	RS232 Interface Signals

Table 7: J2 connector specific signals description.

Table 8 shows the mapping between the FPGA pin locations and the J2 connector pins number and function:

Function	PIN FPGA	Pin number	Pin number	PIN FPGA	Function
TXD1	-	33	34	-	RXD1
IO_40	111	31	32	121	POR_n
IO_39	110	29	30	93	AD_SCLK
IO_CKO_2	91	27	28	106	AD_DIN
IO_38	101	25	26	105	AD_DOUT
IO_37	99	23	24	100	AD_CS_V#
IO_36	92	21	22	97	AD_CS_I#
IO_CKI_4	29	19	20	87	IO_35
IO_CKI_6	89	17	18	88	IO_CKI_5
IO_34	86	15	16	90	IO_CKI_7
IO_41	126	13	14	85	IO_33
IO_31	81	11	12	84	IO_32
IO_29	78	9	10	80	IO_30
IO_27	76	7	8	79	IO_28
IO_25	74	5	6	77	IO_26
IO_23	69	3	4	75	IO_24
IO_21	65	1	2	66	IO_22

Table 8: J2 connector pin function and mapping.

Ref. Des	Connector Part Number	Mates With
J1-J2	Samtec FTS-117-03-F-DV-P • Farnel 1931100	Samtec FFSD-17-D-XX.XX-01-D • Silvestar

Table 9: Connectors specifications

7. Versions Table

The Following table describe the 3 version of pSOC-M10 Board:

GEB Code	Description
171017A1	FPGA 10M08SAE144C8, 32Kbytes EEPROM, 2Mbytes SRAM, 1xRS232, without filters on ADC inputs
171017A2	FPGA 10M08SAE144C8G, 32Kbytes EEPROM, 2Mbytes SRAM, 1xRS232, with filters on ADC inputs
171017A3	FPGA 10M50SAE144C8G, 32Kbytes EEPROM, 2Mbytes SRAM, 1xRS232, witht filters on ADC inputs

Table 10: Versions Table