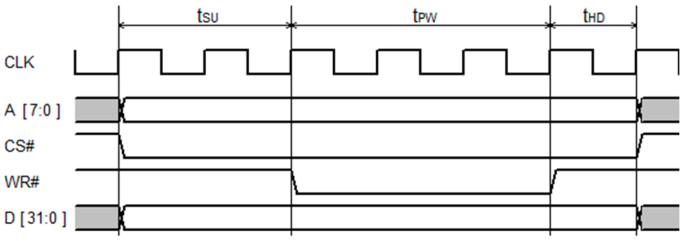
GEB Enterprise S.r.l.
General Electronics Business
Via Rocca di Papa, 21 –00179 Roma, Italy
Email: info@geb-enterprise.com - Web: www.geb-enterprise.com

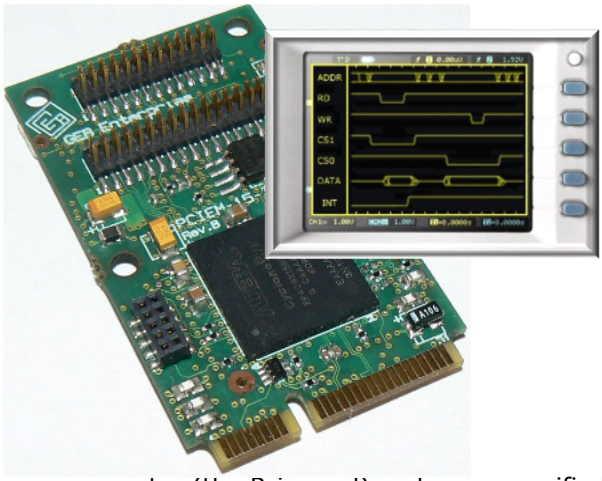
SOPC
System On Programmable Chip

SOPC PCIe: Flexible I/O Bus Interface

Overview

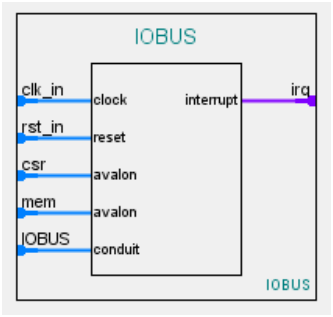
The IOBUS IP is a dynamically reconfigurable asynchronous bus master designed by GEB Enterprise. It supports 8/16/32 Data Bus wide, external interrupts, either fixed latency or variable latency bus cycle.





The IOBUS shall be the bus used for communication between a master (the Pcie card) and an unspecified number of slaves. The bus supports up to 32 Data bits, up to 8 bits address, 2 Chip Select (CS#), Read Enable(RD#), Write Strobe (WR#), Interrupt request (INT#) and an optional Wait signal (WAIT#).

When the IOBUS cycle is started the address and one of the two chip signals are activated on the bus. After the setup time, either the read or the write signal is asserted for the specified time, after which it is de-asserted. The CSL signal is then de-asserted after a specified hold time, after the same time the addresses bus becomes undefined. During Write cycles the data bus follows a timing similar to the addresses bus. The timing can be programmed by host software using a dedicated addressing space (CSR).



On the internal bus side, the IOBUS IP is full compliant with the Altera Avalon Specification, so it can be easily added to any Altera Qsys design. On this side, there are two Avalon Slave Interface, the first one is labeled "MEM" allows acces to external devices. The second interface is labeled "CSR", it implements a configuration space registers that must be used to programming the timings. The CSR allows programming of setup (ts), pulse width (tpw), hold time (th) selectively for Read and Write cycles and also the user can also enable both the interrupt request and the wait signals and their polarity.

Ordering Information

Product Name	GEB Code	Description
PCIE-IOBUS-MS32	141030-01A1	IOBUS IP and QSYS system, targetted on PCIem board. XP and Seven 32 bits drivers and demo
PCIE-IOBUS-MS64	141030-01A3	IOBUS IP and QSYS system, targetted on PCIem board. Seven 64 bits drivers and demo
PCIE-IOBUS-LN64	141030-01A4	IOBUS IP and QSYS system, targetted on PCIem board. Linux 64 bits drivers and demo

GEB Enterprise S.r.l.
General Electronics Business
Via Rocca di Papa, 21 –00179 Roma, Italy
Phone: 06 7827464 Fax: 06 7806894
Email: info@geb-enterprise.com
Web: www.geb-enterprise.com

Document Rev. 0.3.0, Printed 01-04-2015 GEB-Enterprise s.r.l.