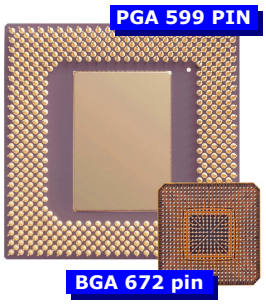
GEB Enterprise S.r.l.
General Electronics Business
Via Rocca di Papa, 21 –00179 Roma, Italy
Email: info@geb-enterprise.com - Web: www.geb-enterprise.com

Test JTAG

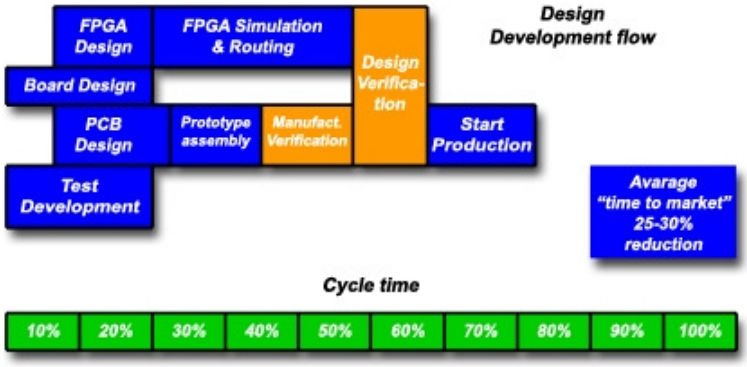
Overview



Due to the increasing PCB complexity and devices density, the impact of new technologies such as array-style IC-packages QFP, BGA,CSP, etc…, have reduced the effectiveness of traditional test methods like functional testing and in-circuit testing (ICT).

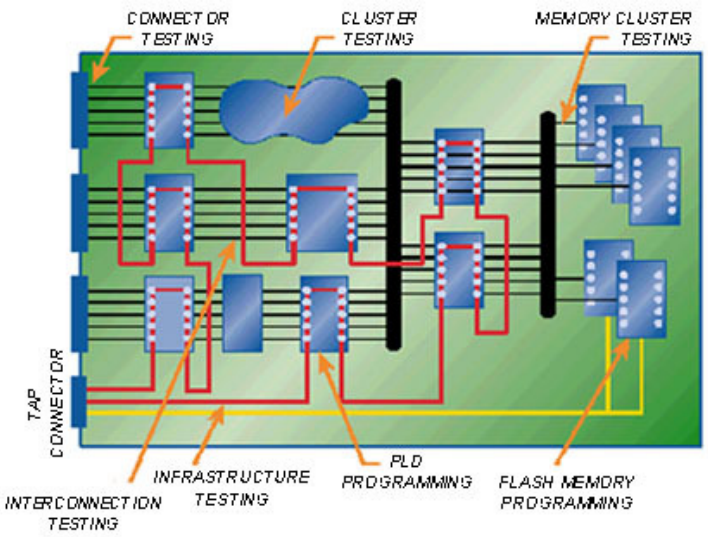
In order to overcome the drawbacks of the traditional test methods, the JTAG (Joint Test Action Group) was set-up by silicon manufacturers representatives with the purpose to select design structures that semiconductor/board makers would incorporate into device designs to test interconnections between Integrated Circuits (ICs) installed on boards, modules and other substrates. The recommendations of this group were adopted as IEEE Standard 1149.1 Test Access Port and Boundary Scan Architecture.

In a traditional design flow, test dedicated to manufacturing faults are not available during the prototypes debug: the consequence is that testing is usually performed with the “unit under test” (UUT) in functional mode, having the simultaneous occurrence of both design faults and manufacturing-related faults.



The JTAG test strategy makes the Design for Testability (DFT) an essential part of the design process: the enterprise adopting JTAG dramatically improves the prototype testing and debug and benefits from the DFT in terms of testing effort reduction, high test coverage on complex PCB’s, and high diagnostic resolution. Once the manufacturing faults are screened by JTAG testing, the prototypes can be tested in functional mode to debug the design.
As a result, the enterprise adopting DFT reduces the prototype cost, improves the product quality and reliability and, last but not least, shortens the time-to-market.

The JTAG test is not limited to the testing of the interconnections (INTER) between components fitted with JTAG interface: It also allows the testing of groups of digital components without JTAG interface (CLUSTER), connected to the card connectors and/or JTAG components. The JTAG pins of the components and connectors are used as a "virtual bed of nails" to stimulate and analyze the CLUSTER responses. This allows functional testing of both simple components such as Gates, Registers, Counters, and complex components such as SRAM, DRAM, FIFO, EEPROM, FLASH, UART, etc ...



The verification of the UUT connectors is performed by the stimulation and capture of its related signals through an optional test fixture which is an electrical and mechanical interface between the JTAG test system and the UUT signals. The test fixture extends the UUT verification to signals having power levels different than standard TTL ones, such as RS232, RS422/RS485, LVDS, Discrete High Voltage (0-15V or 0-28V). The fixture may be realized by connecting standard sensors (sensors JTAG) with Wire Wrap (standard mother board) and/or printed circuit board (custom motherboard).

The manufacturing testing is not the only application for the JTAG standard; it is often adopted by the major suppliers of FPGA using the In-System Programming (ISP) and In-System Configuration (ISC) methodologies. The Flash emulation and programming are additional capabilities of the JTAG standard.

The extension of the JTAG test to the system backplane adds important testing and ISP/ISC capabilities during the debug phase, production, maintenance and updating, even after long time from system installation.
Last but not least, innovative approaches to test "Mixed-Signal" systems (Mixed Analog and Digital) are being developed. Further applications are possible in those cases where the UUT includes a local CPU, selected in functional mode, then the system stimulates and/or checks the state of the board through the Fixture card during the functional tests in "full-speed mode", resident in the firmware of the board itself. This approach provides the customer with important opportunities for test automation in production.

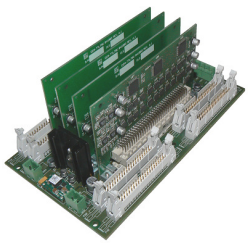
GEB and JTAG

The GEB Enterprise is a development centre "Authorized Application Provider" (AAP) certified by "Technologies (NL)" for JTAG test programs. GEB offers a "turn key" testing solution including JTAG IEEE1149 design, development, implementation and verification. GEB also offers JTAG IEEE1149 courses and training for operators and designers: the courses provide the participants with the capability to develop JTAG Test Programs and Fixtures based on Standard Sensors by themselves.

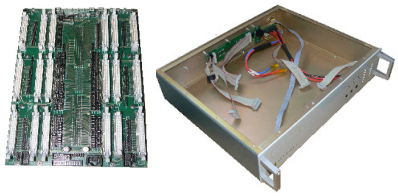
Products and Services

- Consultancy service and support for "Design For Testability" (DFT).
- Test vector development:
  - Trivial, low cost tests: limited to the JTAG components.
  - Standard test: test of JTAG components and clusters (buffer, registers, Sram, DRam, SdRam EEPROM, Flash, Fifo, etc.…)
  - Gold Test,: standard test plus UUT connectors and LVDS, RS232, RS422/RS485, and High Voltage interfaces.
- Test JIG Standard
  - SIMPLEX4, low cost, 316 I/O parallel scan system
  - FDK624 & FDK1560, high performance, Fixture Development Kit
- Full Custom Test JIG
- Courses and Training: Test Programs and Fixtures.
- High Reliable Sensors (BSPIOs) with TTL, LVDS, RS232, RS485, etc…interfaces
  - BSPIO-78TTLU, 78 TTLIO
  - BSPIO-STDIF-1688, 16 RS422/RS485 I/O pair, 8 LVDS I/O pair, 8+8 IN+OUT RS232 channels
  - BSPIO-OPTO1212, 12+12 Opt coupled IN+OUT channels
  - BSPIO-LVDS-39, 39 LVDS I/O pair
  - BSPIO-DIO888, 24 Discrete High Voltage I/O
  - BSPIO-RS485-39, 39 RS422/RS485 I/O pair
  - BSPIO-RELE5, MUX/DEMUX . 5x4, 10x2 o 20x1 channels

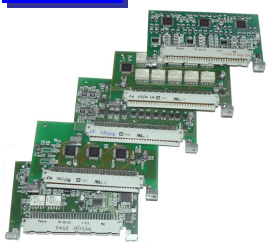
SIMPLEX4-NT Naked version



FDK - Fixture Development KIT



BSPIO



Customer Fixture

GEB Enterprise S.r.l.
General Electronics Business
Via Rocca di Papa, 21 –00179 Roma, Italy
Phone: 06 7827464 Fax: 06 7806894
Email: info@geb-enterprise.com
Web: www.geb-enterprise.com