GEB Enterprise S.r.l.
General Electronics Business
Via Rocca di Papa, 21 –00179 Roma, Italy
Email: info@geb-enterprise.com - Web: www.geb-enterprise.com

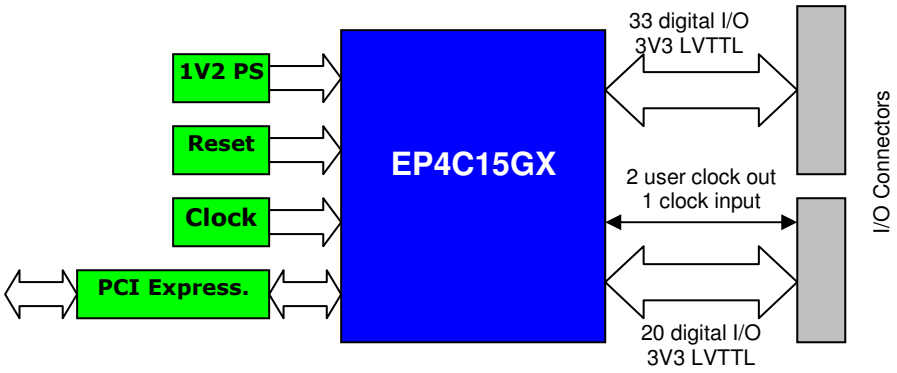
SOPC PCIe System: Dual High Speed SGDMA

Overview

PCI Express family systems are a set of typical basic systems targeted on GEB PCIe boards family (Cyclone IV GX Fpga) which contains all files to make a PCIe subsystem quickly: Configuration files to load on fpga, sopc files, related drivers for multiple OS, simple Demo and test programs. All support files are available in source format. Customer can use the basic system to develops his application hardware and software directly on GEB board, which can be sold in volume at low cost, or may retarget his application on his hardware editing the source files.

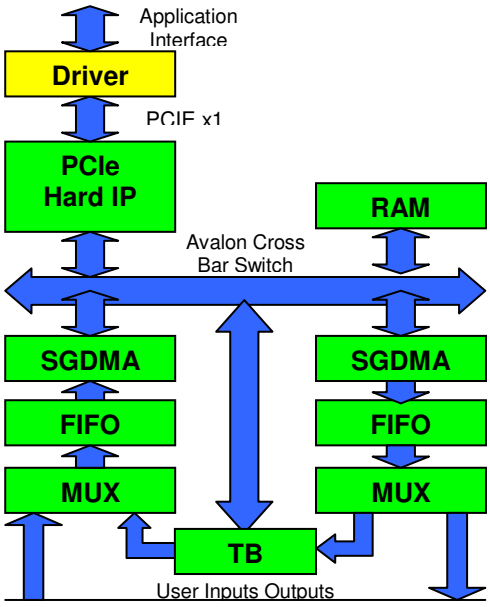
SOPC PCIe Cards Family Features

GEB High Performance System On Card (Sopc-Card) includes, all-in-one, whatever needed to start a PCIe design using the advanced features of Altera CycloneIV-GX family and features a socketed board with an **EP4CGX15** device in a BGA169 package.



Dual High Speed SGDMA Features

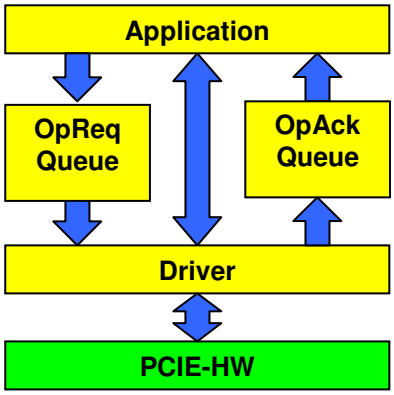
The present basic system is targeted for extreme DMA Application. It includes a system with 2 SGDMA channels whose block diagram can be seen in the right picture.
The two SGDMA channels are configured one in input and one in output. Customer's logics can be connected to user Inputs/Outputs pins. The mux, under control of an Avalon's register, can route the DMA channels ST interface from the I/O pins to TB module. The TB Pheripheral can be used to test the system and measure its performance. The TB peripheral contains a timer, a loopback, a speed programmable pattern checker, and a speed programmable pattern generator. The test mode of TB block can be programmed from Avalon bus. The fifos inside the input output data path allow to mantain the data transfer rate during DMA descriptor and TLB handling in wide DMA. A simple test programm, using the TB block, tests and measures the performance in different driver layouts.
The interface (ST) inside MUX-FIFO-SGDMA chain and iniside SGDMA-PCIe Hard IP are designed to obtain the maximum performance reacheable. The descriptors table are created in local Ram to minimize DMA interblock time.



Driver Architecture

The driver allows direct access to all I/O registers inside Avlon Bus by functions calls. DMA transfer is allowed by an async interface.
For each DMA channel two queue will be created. The first one (OpReq) will be used for Operation Request, the second one (OpAck) for Dma acknowledge. The buffers are created directly in system memory by standard malloc function. The descriptor which contains pointer to user buffer, opcode (Read/Write) and a Requestid, will be enqueued on the request queue. At Dma completion the descriptor will be enqueued on OpAck queue.

- In DMA Read operations the committed buffer will contain the read data and will be used by the customer for the specific data operation.
- In DMA Write operations the buffer will be empty, user application could deallocate it by free or could reuse it for a the next DMA operation.



Customization Service

GEB is available to target PCIe hardware/software subsystem to your needs, integrating your hardware blocks, analyzing and foreseeing the performance, devoloping the SOPC system and drivers on GEB or on Customer Boards. During the design all know-how needed to maintain the system in the next years will be taught to the customers.

Performance

Description	XP 32bits	Seven 64Bits	Linux 64 Bits	Notes
DMA Write, Short Transfer (0.5Mbytes)	154	153	*TBD*	1
DMA Read, Short Transfer (0.5Mbytes)	152	151	*TBD*	1
DMA contemporary Read and Write, Short Transfer (0.5Mbytes)	244	246	*TBD*	1
DMA Write, Long Transfer (128Mbytes)	108	109	*TBD*	1,2
DMA Read, Long Transfer (128Mbytes)	90	92	*TBD*	1,2
DMA contemporary Read/Write, Long Transfer (128Mbytes)	*160*	*158*	*TBD*	1,2
DMA Write, Long Transfer (128Mbytes)	*160*	*160*	*TBD*	1,3
DMA Read, Long Transfer (128Mbytes)	150	151	*TBD*	1,3
DMA contemp. Read/Write, Long Transfer(128Mbytes)	256	252	*TBD*	1,3

Notes:

- 1: All transfer rates are measured in Mbytes/Sec.
- 2: Small driver layout, single buffer
- 3: Medium driver layout, multiple software chained buffer

Ordering Information

Product Name	GEB Code	Description
PCIE-2SGDMA-XP32	120107-02A1	Dual SGDMA QSYS System, Configured XP/32,
PCIE-2SGDMA-732	120107-02A2	Dual SGDMA QSYS System, Configured Seven/32
PCIE-2SGDMA-764	120107-02A3	Dual SGDMA QSYS System, Configured Seven/64
PCIE-2SGDMA-L32	120107-02A4	Dual SGDMA QSYS System, Linux

GEB Enterprise S.r.l.
General Electronics Business
Via Rocca di Papa, 21 –00179 Roma, Italy
Phone: 06 7827464 Fax: 06 7806894
Email: info@geb-enterprise.com
Web: www.geb-enterprise.com