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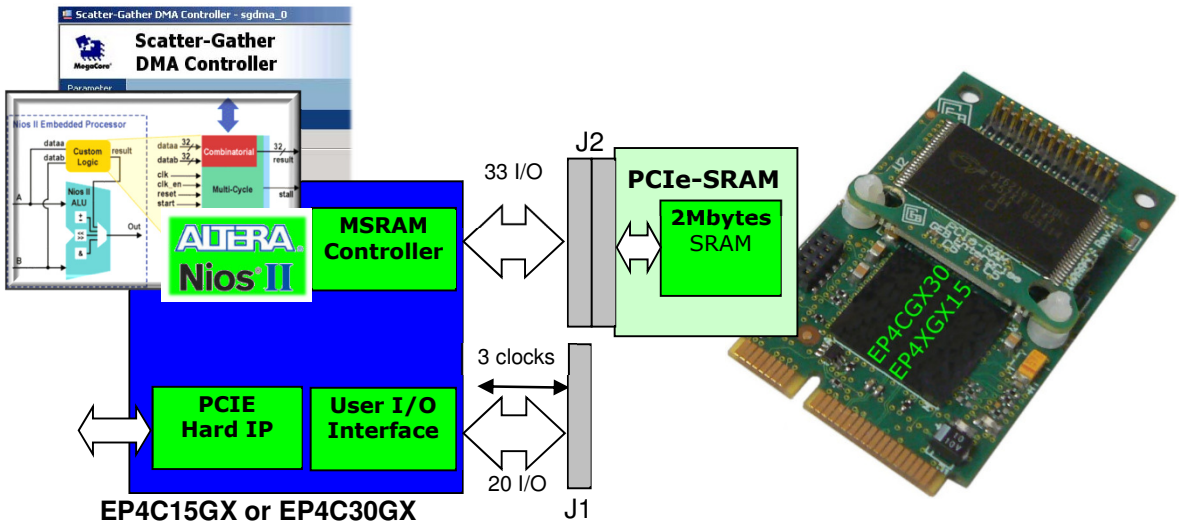
Mini PCI Express Fpga Card with I/O processor

Overview

This product has been thought to make available a smart PCI express I/O able to be a powerful front end. It can host at same time the NIOS microcontroller, the Scatter Gather DMA and hardwired logic with DSP blocks.

Its use allows the interfacing of a lots of sensors, converters and actuators with high performance, both in interrupt response, both when is required a high speed data transfer to/from main memory but also when the data must be processed by DSP or NIOS with its custom instructions before that has been sent to the host cpu.



The NIOS micro controller make available to the developers the handling of I/O interrupts in few tens of ns with deterministic latency, customized instructions that will be able to process your data with a speed and a continuity that are most difficult to reach on the host CPU. Moreover the NIOS can implements a multi channels virtual DMA between lots of high & low speed I/O and the main memory.

The Scatter Gather DMA is able to transfer data between local I/O addressable by J 1 I/O pins and main memory straight in virtual space (That is physically fragmented) at high speed. It can exchange data approximately up to 160MbytesSec. The local NIOS can support the queuing of buffers in the DMA chain, increasing the data transfer speed and minimizing the interrupts to the host.

Multiplexed SRAM Controller

To reduce the number of Fpga I/O pins required to allow the use of the FPGA boards J2, the SRAM board has been designed with a partial multiplexed Address/Data Interface. The user have to interface the SRAM module using a Multiplexed SRAM Controller (MSRAM in the figure) that split 32 bits data access in 2x16 bits data access. To minimize access timing during cache line fill operations, the SRAM LSBits A3-A0 (Avalon A4-A1) addresses bits haven't been multiplexed.

The GEB Enterprise parameterizable MSRAM controller IP can be used to interface the SRAM module to the Avalon bus. It contains the logic needed to split the Avalon bus 32 bits cycle in one send address cycle (when it's needed) and two data cycles. The MSRAM IP is able to tailor the bus cycle timing to the bus speed during compilation.

Ordering Information

Product Name	GEB Code	Description
PCIEm-15K2M-SR	150524A1	Mini PCIe card equipped with EP4CGX15BF14C7N FPGA(15KLE) and 2Mbytes Sram.
PCIEm-30K2M-SR	150524A3	Mini PCIe card equipped with EP4CGX30BF14C6N FPGA (30KLE) and 2 Mbytes Sram.
MSRAM-IP	150415A1	Multiplexed SRam Controller VHDL Source

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