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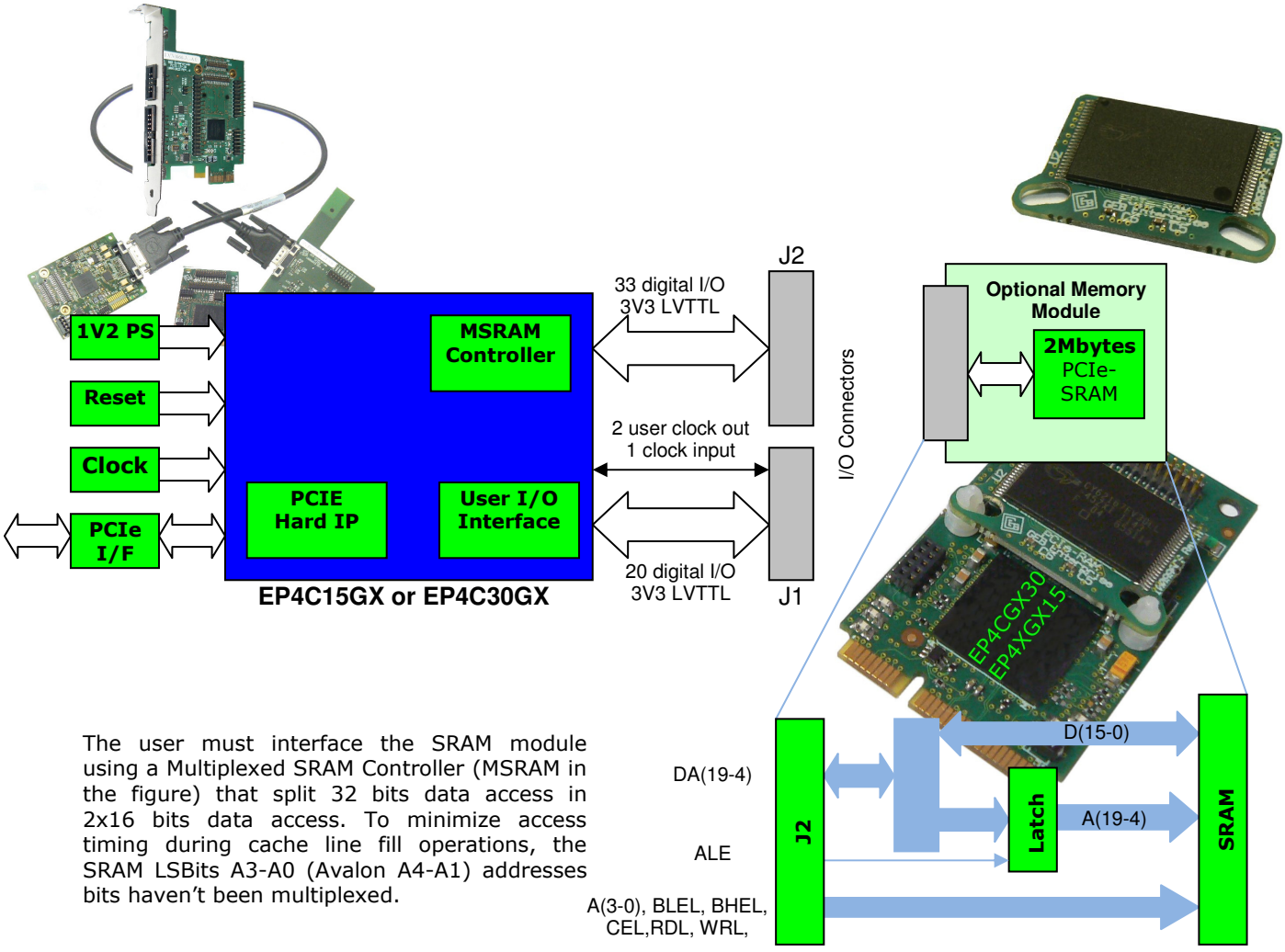
PCI Express 2Mbytes Module for Input Output Boards

Overview

This product is the optional add-on companion board of the PCIed, PCIem, PCIe boards. This is recommended in those cases where a local CPU (e.g. NIOSII core) is required for improving system performances, such as interrupt response time or dedicated pre-processing. The NIOSII processor is able to run up to 200MHz clock frequency, using user defined instructions allowing the user to achieve peak performances which are comparable to an **ATOM CPU at 3.2GHz**. Furthermore, multiple NIOS (up to 4 cores) can be instantiated on the FPGA.

To reduce the number of Fpga I/O pins required to allow the use of the FPGA boards J2, the SRAM board has been designed with a partial multiplexed Address/Data Interface.



The user must interface the SRAM module using a Multiplexed SRAM Controller (MSRAM in the figure) that split 32 bits data access in 2x16 bits data access. To minimize access timing during cache line fill operations, the SRAM LSBits A3-A0 (Avalon A4-A1) addresses bits haven't been multiplexed.

MSRAM Controller

The GEB Enterprise parametric MSRAM controller IP can be used to interface the SRAM module to the Avalon bus. It contains the logic needed to split the Avalon bus 32 bits cycle in one send address cycle (when it's needed) and two data cycles. The MSRAM IP is able to tailor the bus cycle timing to the bus speed during compilation.

The following table contains the map of PCIE-RAM signals on the J2 connector pins

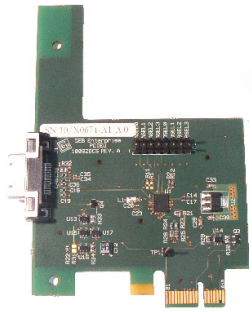
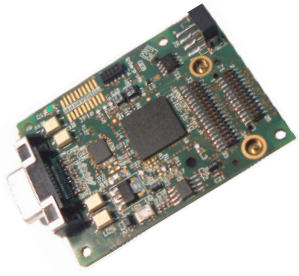
SRAM Function	Default Function	FPGA pin (mini PCIe)	J2 Pin number		FPGA pin (mini PCIe)	Default Function	SRAM Function
Unused	IO51	PIN_A12	1	2	-	+3V3	+3V3
A3	IO49	PIN_A13	3	4	PIN_B11	IO50	A2
BHEL	IO47	PIN_B13	5	6	PIN_D10	IO48	BLEL
WEL	IO45	PIN_C12	7	8	PIN_A6	IO46	A1
DA19	IO43	PIN_C13	9	10	PIN_ D11	IO44	ALE
DA17	IO41	PIN_D12	11	12	PIN_E10	IO42	DA18
DA15	IO39	PIN_D13	13	14	PIN_C6	IO40	DA16
DA13	IO37	PIN_H12	15	16	PIN_F9	IO38	DA14
DA11	IO35	PIN_J13	17	18	PIN_K9	IO36	DA12
DA9	IO33	PIN_K13	19	20	PIN_L9	IO34	DA10
DA8	IO31	PIN_K12	21	22	PIN_H10	IO32	DA7
DA6	IO29	PIN_L13	23	24	PIN_K10	IO30	DA5
DA4	IO27	PIN_M13	25	26	PIN_K11	IO28	A0
CEL	IO25	PIN_N13	27	28	PIN_L11	IO26	RDL
Unused	IO23	PIN_N12	29	30	PIN_M11	IO24	Unused
Unused	IO21	PIN_N11	31	32	PIN_L12	IO22	Unused
Unused	IO20	PIN_N10	33	34	-	GND	GND

Compatibility

The PCIE-RAM is logically compatible with GEB Enterprise PCIe boards family, but due to the connectors matching, it can be hosted just on the following listed board versions:

- PCIem-15-IO Mini-PCIe board, 100801A1 (Fpga EP4CGX15BF14C8N) and 100801A3 (Fpga EP4CGX30BF14C6N)
- PCIed-15-IO PCIe on Cable Downstream Board, 100816A1 (Fpga EP4CGX15BF14C8N) and 100816A2 (Fpga EP4CGX30BF14C6N)
- PCIe-15-IO PCIe Board, Standard PC format, 100815A3 (Fpga EP4CGX15BF14C8N) and 100815A4 (Fpga EP4CGX30BF14C6N)



Ordering Information

Product Name	GEB Code	Description
PCIE-SRAM	100996A1	2Mbytes PCIE-SRAM Module
MSRAM-IP	150415A1	Multiplexed SRam Controller VHDL Source

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