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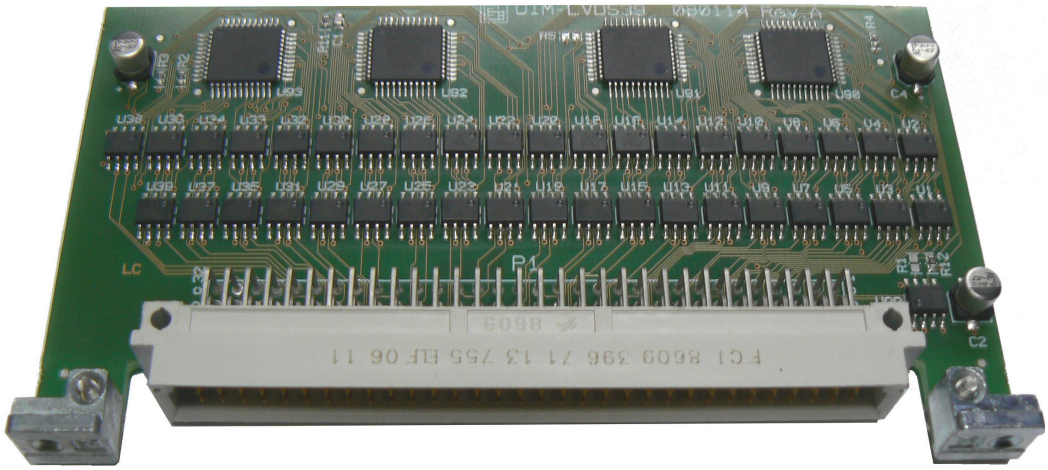
Digital Modules for Boundary Scan Parallel I/O Access

Model: BSPIO-LVDS39



Features

- 39 LVDS I/O channels for interface logic drive and sense
- High reliability DIN41612 I/O connector
- Reliable screw lock brackets
- Size 122mm X 70mm
- 96 bit Boundary-scan Register Length
- Each segment can be independently bypassed
- Medium-speed 10MHz TCK for high reliability at the best cost/performance ratio
- Each LVDS I/O pin is independently programmable for sense, drive, bi-directional, and tri-state operation
- Fully-compatible JTAG/IEEE 1149.1 Test Access Port (TAP)
- Optional LVDS TCK interface can be used in large fixtures to avoid noise and skew problems.
- Full self test capability using internal loopback.

General Description

The BSPIO-LVDS39 provides bi-directional parallel-scan access to up to 39 electrical nodes with LVDS interfaces for the driving and sensing of logic values. This module increases the effectiveness of boundary-scan testing, enabling verification of all board connectors and within logic clusters. The BSPIO-LVDS39 is available in two basic versions, both of them compatible with the standard DIN41612 female connectors in a test fixture. One version, the BSPIO-LVDS39-A1, is primarily intended for test fixtures with few BSPIOsand contains a standard TTL interface on the TAP's TCK signal. This module facilitates boundary-scan interconnection testing using direct connection to the JTAG/IEEE 1149.1 Test Access Port (TAP).
The other version, the BSPIO-LVDS39-A2, is intended for test fixtures with many BSPIOs and contains a balanced LVDS interface on the TAP's TCK signal. This module facilitates boundary-scan interconnection testing using a small interface connection to a JTAG/IEEE 1149.1 TAP. Other low-end versions (ex: 19 channel LVDS) are derived from these two basic models. All BSPIO I/O interfaces have an internal loopback for self test capability.

Functional Description

Test and programming application development tools from JTAG Technologies support automatic integration of the BSPIO-LVDS39 with the target board design by adapter file. This allows the inputs and outputs of the BSPIO-LVDS39 to be driven and sensed via boundary-scan, LVDS interfaces on the target, thereby providing increased scan access. The 39 channels of the BSPIO are capable of operating at a 10 MHz TCK clock rate. The TAP interface available on the DIN41612 connector is the test access port for the module. It can be used to daisy-chain the module to other BSPIO modules (BSPIO-78TTLU, BSPIO-OPTO1212…) or to scan chain on the target board.

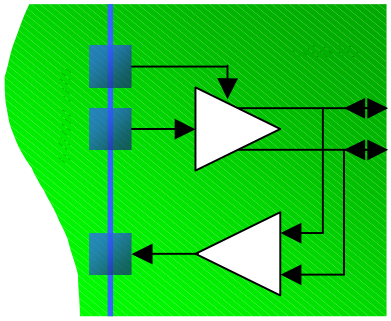


Fig.1 LVDS I/O cells

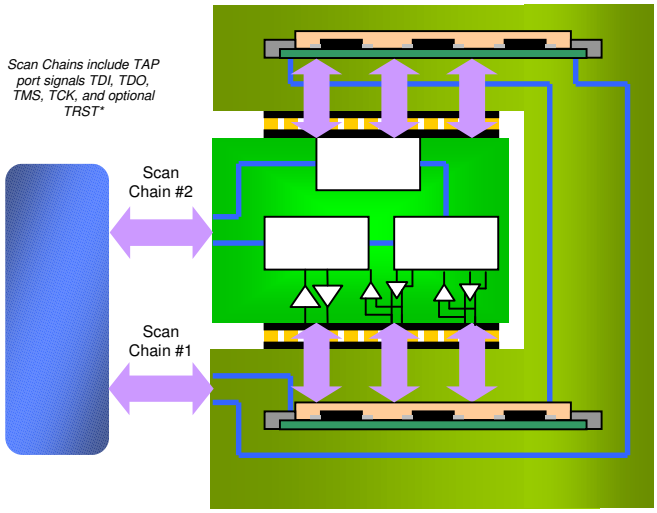


Fig.2 Use of the BSPIO-LVDS39 on the Test Fixture

Specifications

Length of ID Register	32 bits per segment
Length of Boundary-scan Register	96 bits per segment, 3 segments
Maximum Shift Frequency	10MHz
Power Consumption	typ<60mA, max depending on the target I_{OH} and I_{OL}

DC Operating Conditions

LVDS I/O	1<V_{OS}<1.65 V_{TH}/$V_{TL=+/-}$100mV
TAP (*1)	All V_{IL}<0.8V V_{IH}>2.0V
TAP TCK(*2)	1<V_{OS}<1.65 V_{TH}/$V_{TL=+/-}$100mV

(*1) Not Applicable to TCK version A2
(*2) Applicable to TCK version A2

Ordering Information

GEB P.N. (*)	Description
BSPIO-LVDS39-A1/A2	39 LVDS I/O
BSPIO-LVDS39-A3/A4	19 LVDS I/O

(*) Odd-numbered versions (A1,A3…) have LVTTL level on TCK input, Even numbered versions (A2,A4…) have balanced LVDS levels on TCK input

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