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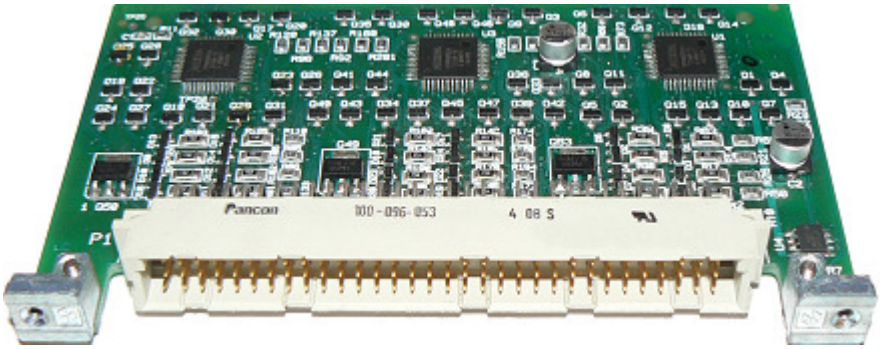
Digital Modules for Boundary Scan Parallel I/O Access

Model: BSPIO-DIO888



Features

- 24 Discrete High Voltage discrete I/O channels for interface logic drive and sense
- 16 I/O TTLs, drives 3.3V logic, 5V tolerant
- High reliability DIN41612 I/O connector
- Reliable screw lock brackets
- Size 122mm X 70mm
- Discrete I/O organized in 3 segment of 8 pins each
- 96 bit Boundary-scan Register Length
- Each segment can be independently bypassed
- Medium-speed 10MHz TCK for high reliability at the best cost/performance ratio
- Each I/O pin is independently programmable for sense, drive, bi-directional, and tri-state operation
- Fully-compatible JTAG/IEEE 1149.1 Test Access Port (TAP)
- Operating power 3.3V, 5.0V
- Optional LVDS TCK interface can be used in large fixtures to avoid noise and skew problems.
- Full self test capability using internal loopback.

General Description

The BSPIO-DIO888 provides bi-directional parallel-scan access to up to 40 electrical I/O nodes, 24 with high voltage level and 16 nodes with standard TTL level, for the driving and sensing of logic values. This module increases the effectiveness of boundary-scan testing, enabling verification of board edge and on-board connectors and within logic clusters. The BSPIO-DIO888 is available in two basic versions, both of them compatible with standard DIN41612 female connectors in a test fixture. One version, the BSPIO- DIO888-A1, is primarily intended for test fixtures with few BSPIOs, and contains a standard TTL interface on the TAP's TCK signal. This module facilitates boundary-scan interconnection testing using direct connection to a JTAG/IEEE 1149.1 Test Access Port (TAP).
The other version, the BSPIO-DIO888-A2, is intended for test fixtures with many BSPIOs and contains a balanced LVDS interface on the TAP's TCK signal. This module facilitates boundary-scan interconnection testing using a small interface connection to a JTAG/IEEE 1149.1 TAP. All BSPIO I/O interfaces have an internal loopback to ensure the self test capability.

Functional Description

Test and programming application development tools from JTAG Technologies support automatic integration of the BSPIO-DIO888 with the target board design by adapter file. This allows the inputs and outputs of the BSPIO- DIO888 to be driven and sensed via a boundary-scan discrete interface on the target, thereby providing increased scan access. The 24 discrete I/O interfaces are grouped into three banks, each bank is composed of 8 I/O open collectors with pull up resistors that can be enabled by the boundary scan cell at a VOH voltage defined in the connection stage (hardwired option). *See Fig. 1*

The 40 channels of the BSPIO are capable of operating at a 10 MHz TCK clock rate. The TAP interface available on DIN41612 connector is the test access port for the module. It can be used to daisy-chain the module to other BSPIO modules (BSPIO-78TTLU, BSPIO-STDIF…) or to the scan chain on the target board. *See Fig. 2*.

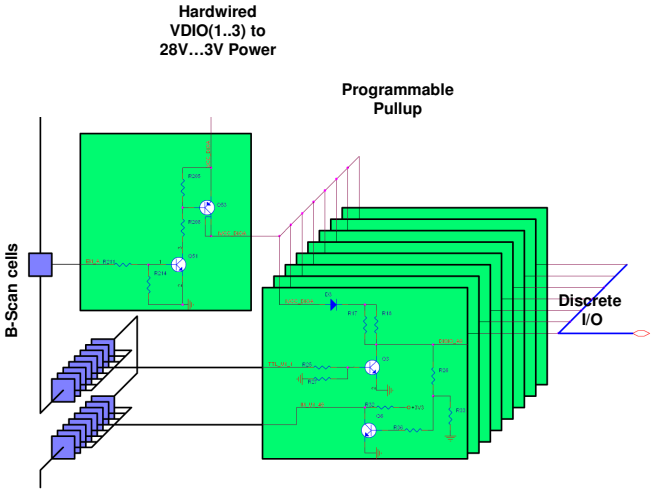


Fig.1 Discrete I/O cells

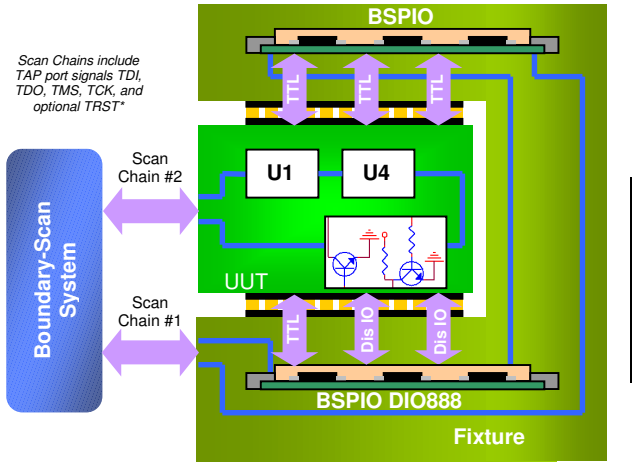


Fig.2 Use of the BSPIO-DIO888 on the Test Fixture

Specifications

Length of ID Register	32 bits per segment
Length of Boundary-scan Register	96 bits per segment, 3 segments
Maximum Shift Frequency	10MHz
Power Consumption	typ<80mA, max depending on the target I_{OH} and I_{OL}

DC Operating Conditions

TTL I/O	V_{IL}<0.8V V_{IH}>2.0V V_{IL}<0.4V V_{OH}>2.4V
Discrete I/O	V_{IL}<2.0V V_{IH}>4.0V V_{OL}<0.4V (IOL =50mA) V_{OH}> VDIO-1.2-Rs*I_{OH} V_{OH}>19.5V (VDIO=28V IOH=10mA) V_{OH}>12.0V (VDIO=28V IOH=20mA) Max I_{OH}=24mA (Continuous) Max I_{OH}=50mA (Duty Cycle 50%, 50mS max)
TAP (*1)	V_{IL}<0.8V V_{IH}>2.0V V_{OL}<0.4V V_{OH}>2.4V
TAP TCK(*2)	1<V_{OS}<1.65 V_{TH}/$V_{TL=+/-}$100mV

(*1) Applicable to TCK odd-numbered versions (A1,A3…)
(*2) Applicable to TCK even-numbered versions (A2,A4…)

Ordering Information

GEB P.N. (*)	Description
BSPIO-DIO888-A1/A2	24 Discrete I/O (3 Groups of 8 I/Os), 16 TTL I/O, Rs=750Ω
BSPIO-DIO888-A3/A4	16 Discrete I/O (2 Groups of 8 I/Os), 16 TTL I/O, Rs=750Ω
BSPIO-DIO888-A5/A6	8 Discrete I/O (1 Groups of 8 I/Os), 16 TTL I/O, Rs=750Ω

(*) Odd-numbered versions (A1, A3…) have LVTTL level on TCK input, Even numbered versions (A2,A4…) have balanced LVDS levels on TCK input

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